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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,797	06/18/2001	Michael J. Miller	IDT-1654	4392

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EXAMINER	
ANDERSON, MATTHEW D	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,797	MILLER ET AL.	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24* is/are allowed.

6)☒ Claim(s) *1-13 and 16-23* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/18/01, 3/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because figure 1 should be designated by a legend such as -- Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9-13, 16-17, 19-20, and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) and Hariguchi (US Patent # 6,307,855).

4. With respect to claim 1, AAPA discloses:

a plurality of content addressable memory (CAM) blocks, as shown by item 202 in figure 2;

a priority encoder coupled to receive the hit signals routed by the configurable switching circuit, the priority encoder being configured to provide an output hit signal representative of an asserted hit signal having a highest priority in the first order, as shown by item 230 in figure 2.

5. AAPA teaches all other limitations as discussed above, but fails to specifically disclose the following which is taught by Hariguchi.

each CAM block configured to provide a hit signal and an index signal in response to an applied address, as shown in figure 6 by each Cam block being connected to a entry hit line and mask index register line;

a plurality of programmable storage elements configured to store a plurality of routing values, and a configurable switching circuit coupled to receive the hit signals from the CAM blocks and the routing values from the programmable storage elements, wherein the configurable switching circuit routes the hit signals in a first order in response to the routing values, by teaching in figure 8 of a routing engine 400 containing a routing table, ARP table and routing result generator which sends the routing result back to the header translator to determine the port used;

a first multiplexer configured to route one of the routing values from the programmable storage elements as an index routing value in response to the output hit signal; and a second multiplexer configured to route an index signal from one of the CAM blocks as an output index value in response to the index routing value, as shown by the circuitry in figure 7-8.

6. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Hariguchi before him at the time the invention was made, to modify the CAM system taught by AAPA, to include the routing index register circuitry of the CAM system of Hariguchi, in order to provide fast, parallel route look-up, as taught by Hariguchi.

7. With respect to claim 2, AAPA discloses a static random access memory (SRAM) array, wherein the index routing value and the output index value are provided to access the SRAM array, as taught in paragraph 9.

8. With respect to claim 3, AAPA discloses wherein the SRAM array includes a plurality of SRAM blocks corresponding with the CAM blocks, as taught in paragraphs 9-12.

9. With respect to claim 4, Hariguchi discloses wherein the configurable switching circuit comprises a plurality of multiplexers, each corresponding with one of the CAM blocks, and each being coupled to receive all of the hit signals from the CAM blocks, as shown by the comparator 210 in figure 5 attached to each CAM cell.

10. With respect to claim 5, Hariguchi discloses wherein each of the programmable storage elements is coupled to a corresponding one of the multiplexers, wherein each of the multiplexers routes one of the hit signals in response to the routing value stored in the corresponding programmable storage element, as shown in figure 7-8.

11. With respect to claim 6, AAPA discloses wherein one or more of the CAM blocks is designated to store only prefixes having a first length, and one or more of the CAM blocks is designated to store only prefixes having a second length, different than the first length, as shown in figure 2.

12. With respect to claim 7, AAPA discloses wherein one or more of the CAM blocks stores is designated to store only prefixes having a third length, different than the first and second lengths, as shown in figure 2.

13. With respect to claim 9, AAPA discloses wherein the asserted hit signal having the highest priority and the output index value originate in the same CAM block, as taught by the longest prefix matching algorithm in figure 2.

14. With respect to claim 10, Hariguchi discloses wherein the system includes thirty-two CAM blocks, as recited in column 9, line 9.

15. With respect to claim 11, AAPA discloses wherein the addresses are Classless Inter-Domain Routing (CIDR) addresses, as taught in paragraph 9.

16. With respect to claim 12, AAPA discloses wherein a first set of the CAM blocks is designated to store a set of prefixes of a first priority chain, wherein each of the CAM blocks in the first set is designated to store a corresponding one of the prefixes of the first priority chain, by teaching in paragraph 8 that each of CAM sub-arrays 208-228 is dedicated to store prefixes of a predetermined length.

17. With respect to claim 13, AAPA discloses wherein a second set of the CAM blocks is designated to store a set of prefixes of a second priority chain, wherein each of the CAM blocks in the second set is designated to store a corresponding one of the prefixes of the second priority chain, by teaching in paragraph 8 that each of CAM sub-arrays 208-228 is dedicated to store prefixes of a predetermined length.

18. With respect to claim 16 AAPA discloses:

storing prefixes having a first length in a first set of one or more content addressable memory (CAM) blocks, as shown by item 202 in figure 2;

storing prefixes having a second length in a second set of one or more CAM blocks, the second length being different than the first length, as shown by item 2 in figure 202;

receiving an input address with the first and second sets of CAM blocks, as shown by item 201 in figure 2;

generating a hit signal and an index signal with each of the CAM blocks in the first and second sets of CAM blocks in response to the input address, as taught in paragraph 9;

routing the hit signal generated by each of the CAM blocks to a priority encoder in an order determined by the routing values, as taught in paragraph 9;

generating an output hit signal with the priority encoder in response to the hit signals, as taught in paragraph 9.

19. AAPA though, while teaching all other limitations, as discussed above, does not specifically disclose storing a plurality of routing values in a programmable register, and routing one of the routing values as an index routing value in response to the output hit signal, and routing one of the index signals as an output index value in response to the index routing value.

20. Hariguchi teaches in figure 8 of a routing engine 400 containing a routing table, ARP table and routing result generator which sends the routing result back to the header translator to determine the port used.

21. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Hariguchi before him at the time the invention was made, to modify the CAM system

taught by AAPA, to include the routing index register circuitry of the CAM system of Hariguchi, in order to provide fast, parallel route look-up, as taught by Hariguchi.

22. With respect to claim 17, Hariguchi discloses further comprising using the index routing value and the output index value to address a memory array, as shown in figure 8.

23. With respect to claim 19, AAPA discloses wherein the output hit signal is representative of an asserted hit signal having a highest priority, as taught by the longest prefix matching algorithm in figure 2.

24. With respect to claim 20, AAPA discloses wherein the asserted hit signal having the highest priority and the output index value originate in the same CAM block, as taught by the longest prefix matching algorithm in figure 2.

25. With respect to claim 22, AAPA discloses wherein the input address is a Classless Inter-Domain Routing (CIDR) address, as taught in paragraph 9.

26. With respect to claim 23, AAPA discloses storing prefixes having a third length, different than the first and second lengths, in a third set of one or more CAM blocks. receiving the input address with the third set of CAM blocks; and generating a hit signal and an index signal with each of the CAM blocks in the third set of CAM blocks in response to the input address, as taught in paragraph 9 and figure 2.

27. Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hariguchi, and Pereira et al. (US Patent # 6,249,467).

28. AAPA and Hariguchi teach all other limitations, as discussed above, but fail to specifically disclose wherein one or more of the CAM blocks are initially designated as spare CAM blocks that do not store prefixes unless one of the other CAM blocks becomes full. Pereira et al. teach in figure 1 of a spare Cam block used when other blocks are full.

29. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Hariguchi, and Pereira et al. before him at the time the invention was made, to modify the CAM system taught by AAPA and Hariguchi, to include the spare blocks of the CAM system of Pereira et al., in order to replace defective CAM rows, as taught by Pereira et al..

30. Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hariguchi, and Nusinov et al. (US Patent # 5,467,319).

31. AAPA and Hariguchi teach all other limitations, as discussed above, but fail to specifically selecting the routing values such that the hit signals associated with the first set of CAM blocks are routed consecutively to the priority encoder, and the hit signals associated with the second set of CAM blocks are routed consecutively to the priority encoder. Nusinov et al. teach in column 3, lines 50-55, a plurality of first CAM cells serially coupled for propagating match signals from least significant to most significant first CAM cells.

32. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Hariguchi, and Nusinov et al. before him at the time the invention was made, to modify the CAM system taught by AAPA and Hariguchi, to include the consecutive routing of the CAM system of Nusinov et al., in order to reduce propagation delays and minimize track routing, as taught by Nusinov et al..

Allowable Subject Matter

33. Claim 24 is allowed.

34. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. The following is an examiner's statement of reasons for allowance: the prior art does not teach or suggest sets of prefixes of different priority chains being stored in a common CAM block.

36. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (571) 272-4177. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew D. Anderson
Primary Examiner
Art Unit 2186